PATENT
Attorney Docket No.3543US (97-952)

NOTICE OF EXPRESS MAILING

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Person making Deposit: Matthew Wooton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Serial No.:	09/277,893	Group Art Unit No.:	2815
Filing date:	March 29, 1999	Examiner:	P. Brock, II
For (title):	SEMICONDUCTOR FUSES, SEMICONDUCTOR DEVICES CONTAINING THE SAME, AND METHODS OF MAKING AND USING THE SAME		

TRANSMITTAL OF BRIEF ON APPEAL (PATENT APPLICATION — 37 C.F.R. § 192)

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

1. Transmitted herewith in triplicate is the BRIEF ON APPEAL in this application with respect to the Notice of Appeal filed on November 6, 2002.

2. STATUS OF APPLICATION
This application is on behalf of
- [x] other than a small entity
- [ ] small entity

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 C.F.R. § 1.17(f) the fee for filing the Appeal Brief is:

[ ]	small entity status	$160
[x]	other than a small entity	$320

4. EXTENSION OF TIME

[ ] A petition for Extension of Time for a month extension of time for filing the Appeal Brief is enclosed.

5. FEE PAYMENT

[x] Check No. 3532 is enclosed in payment of the fee for filing the Appeal Brief plus any extension of time for which a petition has been filed.
[ ] Please charge this fee to deposit account No. 20-1469 (a duplicate copy of this notice is enclosed--see below).

Any additional appeal fees which are not otherwise submitted herewith or which are insufficient should be charged to deposit account no. 20-1469. A duplicate copy of this notice is enclosed. Please address all communications in connection with this appeal to the address indicated below.

Respectfully submitted,

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Date: January 6, 2003
Enclosures: As identified above
BGP/djp

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Kenneth W. Marr

Serial No.: 09/277,893

Filed: March 29, 1999

For: SEMICONDUCTOR FUSES, SEMICONDUCTOR DEVICES CONTAINING THE SAME, AND METHODS OF MAKING AN USING THE SAME

Examiner: P. Brock, II

Group Art Unit: 2815

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BRIEF ON APPEAL

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is submitted in TRIPLICATE pursuant to 37 C.F.R.§ 1.192(a) and in the format required by 37 C.F.R. § 1.192(c) and with the fee required by 37 C.F.R. § 1.17(c).

(1) REAL PARTY IN INTEREST

U.S. Serial No. 09/277,893, the patent application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc. ("Assignee"). The assignment has been recorded with the United States Patent & Trademark Office ("Office") at Reel No. 9878, Frame No. 0785. Accordingly, Micron Technology, Inc. is the real party in interest to the referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

On November 26, 2002, a Notice of Appeal was filed in U.S. Application serial no. 09/702,583, which was filed on October 31, 2000, and is a divisional of the above-referenced application. Neither Appellant, Appellant's representative, nor Assignee is aware of any pending appeal or interference which would directly affect, be directly affected by, or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF CLAIMS

Claims 17-33, 50-72, and 74-101 are currently pending in the above-referenced patent application. Claims 17-33, 50-72, and 74-101 stand rejected.

Claims 1-16, 34-49, and 73 were previously cancelled without prejudice or disclaimer.

No claims have been allowed.

The rejections of claims 17-33, 50-72, and 74-101 are being appealed.

(4) STATUS OF AMENDMENTS

Claims 1-101 were initially filed in the above-referenced application.

A Restriction Requirement was made on October 3, 2000. Pursuant to an election without traverse to prosecute claims 17-33 and 50-101 in a response dated October 19, 2000, claims 1-16 and 34-49 were withdrawn from consideration. Claims 1-16 and 34-49 were subsequently canceled, without prejudice or disclaimer, in an Amendment dated February 26, 2001.

A first Office Action on the merits was mailed on December 21, 2000. Each of claims 17-33 and 50-101 was rejected in the first Office Action. In a responsive Amendment, which was dated February 26, 2001, several claim amendments were presented, along with reasoning as to the allowability of the amended claims over the art that had been relied upon in the first Office Action. In particular, claims 17, 50, and 71 were amended, as were several dependent claims. In addition, claim 73 was canceled without prejudice or disclaimer.

Next, a first Final Office Action was mailed on April 12, 2001. Again, each of the claims that remained pending and under consideration in the above-referenced application was rejected, including claims 17-33, 50-72, and 74-101. In response, an Amendment Under 37 C.F.R. § 1.116 was filed on May 29, 2001, in which further explanations as to the allowability of claims 17-33, 50-72, and 74-101 were provided and another amendment to claim 71 was proposed.

In an Advisory Action dated June 7, 2001, several of the claim rejections were maintained. A Request for Continued Examination was subsequently filed on June 12, 2001.

A third, non-final Office Action was mailed on June 12, 2001. In the third Office Action, each of claims 17-33, 50-72, and 74-101 was again rejected. On October 17, 2001, another response was filed. No additional claim amendments were made in that response.

The Office replied with a second Final Office Action on November 27, 2001. The response thereto, an Amendment Under 37 C.F.R. § 1.116 which was filed on January 11, 2002, included proposed amendments to each of independent claims 17, 50, and 71. In an Advisory Action, which was mailed on January 29, 2002, the Office refused to enter the proposed claim amendments. In order to cause the proposed claim amendments to be entered, a second Request for Continued Examination was filed on February 7, 2002.

On April 16, 2002, another non-final Office Action, the fifth Office Action in the above-referenced application, was mailed. Again, each of claims 17-33, 50-72, and 74-101 was rejected. Again, the Office remained unconvinced by the reasoning provided in the response thereto, which was dated July 16, 2002.

As a result, the Office mailed a sixth, Final Office Action on August 21, 2002. The previous reasoning as to the patentability of claims 17-33, 50-72, and 74-101 was reiterated and enhanced in a response dated October 17, 2002.

Nonetheless, in an Advisory Action that was mailed on October 31, 2002, the rejections of claims 17-33, 50-72, and 74-101 were maintained.

Accordingly, a Notice of Appeal was filed in the above-referenced application on November 6, 2002.

(5) SUMMARY OF THE INVENTION

The above-referenced application describes and claims methods for fabricating fuses. Fuses that are fabricated in accordance with the inventive methods include terminals with a lower layer of conductive material, such as a metal or conductively doped polysilicon, and an upper layer that comprises a metal silicide or polycide. Page 4, lines 14-16; page 7, lines 9-12; FIGs. 7 and 8. A central, or fusible, region of the fuse, which is located between two terminals thereof, comprises the metal silicide or polycide but not the other conductive material. Page 4, lines 14-16; page 7, lines 12-15; FIGs. 7 and 8.

In fabricating the fuse, a layer of the conductive material may be deposited adjacent an insulative structure, such as a field oxide region of a semiconductor device structure. Page 5, lines 8-10; page 9, lines 9-15; FIG. 3. The layer of conductive material is patterned to define at least two discrete spaced apart regions, which are located adjacent to the insulative structure. Page 4, line 27, to page 5, line 1; page 5, lines 10-12; page 9, line 16, to page 10, line 14; FIG. 4. The underlying insulative structure is, therefore, exposed between the spaced apart regions of the layer of conductive material. Page 5, lines 12-14; page 10, lines 7-10; FIG. 4.

A layer of the metal silicide or polycide is formed over the layer of conductive material and on the portion of the insulative structure which is exposed between the spaced part regions of the layer of conductive material. Page 5, lines 15-19; page 10, line 15, to page 11, line 6; FIG. 5. The layer of metal silicide or polycide is patterned to define the upper layers of the fuse terminals and the central region of the fuse. Page 5, lines 19-25; page 11, line 7, to page 12, line 3; FIG. 6. The material volume of each terminal exceeds the material volume of the central region of the

fuse. Page 5, lines 25-27. The central region of the fuse may also be narrower than the terminals thereof. Page 11, lines 17-19.

(6) ISSUES

(A) Whether the drawings of the above-referenced application comply with the requirements of 37 C.F.R. § 1.121(a)(6) by depicting subject matter which is supported by the specification that was originally filed in the above-referenced application;

(B) Whether the drawings of the above-referenced application comply with the requirements of 37 C.F.R. § 1.83(a) by appropriately depicting subject matter which is recited in the claims;

(C) Whether the specification of the above-referenced application provides proper antecedent basis for the subject matter recited in the claims, in compliance with 37 C.F.R. § 1.75(d)(1) and M.P.E.P. § 608.01(o);

(D) Whether claims 17-33, 50-72, and 74-101 are allowable under 35 U.S.C. § 112, first paragraph, for describing the inventive subject matter in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention;

(E) Whether claims 17, 19-24, and 26-33 recite subject matter which is patentable under 35 U.S.C. § 103(a) over U.S. Patent 5,185,291 to Fischer et al. (hereinafter "Fischer") in view of U.S. Patent 5,712,206 to Chen (hereinafter "Chen");

(F) Whether claim 18 recites subject matter which is allowable under 35 U.S.C. § 103(a) over Fischer and Chen and, further, in view of Japanese Patent No. 59-154,038 to Mitani (hereinafter "Mitani");

(G) Whether claim 25 is allowable under 35 U.S.C. § 103(a) as reciting subject matter which is patentable over Fischer and Chen and, further, in view of U.S. Patent No. 5,231,056 to Sandhu (hereinafter "Sandhu");

(H) Whether claims 50, 51, 55-60, and 62-68 are allowable under 35 U.S.C. § 103(a) as reciting subject matter which is allowable over the combination of Fischer in view of Mitani and Chen;

(I) Whether claims 52-54, 69, and 70 recite subject matter which is patentable under 35 U.S.C. § 103(a) over the combination of Fischer, Mitani, Chen, and U.S. Patent 5,242,859 to Degelormo et al. (hereinafter "Degelormo");

(J) Whether claim 61 is allowable for reciting subject matter which, under 35 U.S.C. § 103(a), is patentable over the combination of Fischer, Mitani, Chen, and Sandhu;

(K) Whether, under 35 U.S.C. § 103(a), claims 71, 74-86, 88-96, and 101 are patentable over Mitani, Fischer, and Chen;

(L) Whether claim 72 is patentable, under 35 U.S.C. § 103(a), for reciting subject matter which is allowable over the combination of Mitani, Fischer, Chen, and Degelormo;

(M) Whether claim 87 recites subject matter which is patentable under 35 U.S.C. §103(a) over the combination of Mitani, Fischer, Chen, and Sandhu; and

(N) Whether claims 97-100 recite subject matter which is patentable under 35 U.S.C. § 103(a) as being nonobvious over the combination of Mitani, Fischer, Chen, and U.S. Patent 6,069,055 to Ukeda et al. (hereinafter "Ukeda").

(7) GROUPING OF CLAIMS

Group 1: Claims 17-33:

Claims 17-33 are grouped together. Claim 17 is the most generic claim of Group 1. For purposes of this appeal, claims 18-33 stand with claim 17, but claims 18 and 25 do not fall with claim 17.

Group 2: Claims 50-70:

Claims 50-70 are grouped together. Claim 50 is the most generic claim of Group 2. For purposes of this appeal, claims 51-70 stand with claim 50, but claims 52-54, 61, 69, and 70 do not fall with claim 50.

Group 3: Claims 71, 72, and 74-101:

Claims 71, 72, and 74-101 are grouped together. Claim 71 is the most generic claim of Group 3. For purposes of this appeal, claims 72 and 74-101 stand with claim 72, but claims 72, 87, and 97-100 do not fall with claim 71.

(8) ARGUMENT

(A) Objection Under 37 C.F.R. § 1.121(a)(6)

The Drawings have been objected to under 37 C.F.R. § 1.121(a)(6) for introducing new matter into the above-referenced application. In particular, it has been asserted that the originally filed specification does not support the illustration of regions of a first conductive material which are laterally spaced apart and discrete from one another.

Page 4, line 27, to page 5, line 1 of the originally filed specification provides that the polysilicon of or that underlies the terminals "is disposed on [an] insulative structure in discrete regions of portions that are substantially isolated from one another."

In addition, page 9, line 27, to page 10, line 1 of the originally filed specification describes regions 14a and 14b that are laterally spaced apart from one another, and which may be laterally discrete from one another. Notably, regions 14a and 14b are depicted in originally filed FIGs. 6-8. When taken in view of the statement that "*[a]ny previously unpatterned portions* of layers 14 and 12 *may* also *be patterned,* ***as necessary,*** to further define gate 20 and fuse 22 . . ." (emphasis supplied), which appears at page 11, lines 9-11, of the originally filed specification, it is clear that the originally filed specification provides support for spaced apart regions 14a and 14b that are also laterally discrete from one another.

Accordingly, the 37 C.F.R. § 1.121(a)(6) objection to the drawings should be reversed.

(B) Objection Under 37 C.F.R. § 1.83(a)

The drawings have also been objected to under 37 C.F.R. § 1.83(a) for failing to show each and every element recited in the claims. Specifically, it has been asserted that the "laterally discrete spaced apart regions" of a first conductive layer have been omitted from the drawings. Such an element is clearly depicted in each of FIGs. 6-8, in which the laterally discrete spaced apart regions are identified by reference characters 14a and 14b. Moreover, FIG. 4A, which was provided merely to clarify subject matter which was already described in the originally filed specification, provides another view of the subject matter shown in FIG. 4, in which the portions of the first conductive layer that remaining following patterning thereof are laterally discrete and spaced apart from one another.

Therefore, the 37 C.F.R. § 1.83(a) objection to the drawings should be reversed.

Notably, on page 2 of the Final Office Action dated August 21, 2002, a threat was made to abandon the above-referenced application if FIG. 4A was not removed from the drawings.

(C) Objection to the Specification

The specification has been objected to under 37 C.F.R. § 1.75(d)(1) and M.P.E.P. § 608.01(o) for failing to provide proper antecedent basis for the subject matter which is recited in the claims. Again, it has been asserted that the recitation of "laterally discrete spaced apart regions" of a first layer of conductive material lacks support in the originally filed specification.

Looking to page 4, line 27, to page 5, line 1, and to page 9, line 27, to page 10, line 1, of the originally filed specification, it is clear that the spaced apart regions 14a and 14b, which are shown in originally filed FIGs. 6-8, may be laterally discrete and spaced apart from one another.

Accordingly, the objections to the specification should be reversed.

(D) Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 17-33, 50-72, and 74-101 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Again, the spaced apart regions 14a and 14b which are described, for example, at page 9, line 16, to page 10, line 7, of the originally filed specification are shown in originally filed FIGs. 6-8 as being laterally discrete from one another. Although the accompanying descriptive text does not itself explain that these regions are laterally discrete from one another, the originally filed drawings, particularly FIGs. 4-8, do not depict regions 14a and 14b as being anything other than laterally discrete from each other. Moreover, page 4, line 27, to page 5, line 1, or the originally filed specification clearly provides that the polysilicon may disposed as discrete regions or portions that are substantially isolated from one another. Further, page 11, lines 9-11 of the originally filed specification clearly indicate that, following the patterning of a layer 16 which has been formed over spaced apart regions 14a and 14b, it may not be necessary to further pattern the remaining portions of layer 14.

Thus, the originally filed specification clearly indicates that the spaced apart regions 14a and 14b may be laterally discrete from one another. Any other interpretation of the described subject matter could only be conjecture based on a series of assumptions.

Accordingly, the originally filed specification describes the claimed subject matter in such a way as to reasonably convey to one of ordinary skill in the art that, at the time the above-referenced application was filed, the inventor was in possession of the claimed invention. Therefore, the 35 U.S.C. § 112, first paragraph rejection of claims 17-33, 50-72, and 74-101 should be reversed.

(E) Rejections Under 35 U.S.C. § 103(a)

(1) Pertinent Law

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(2) References Relied Upon

Fischer

Fischer teaches a fuse for use in a semiconductor device structure, as well as a process for fabricating the fuse. The fuse of Fischer, which is disposed over an insulative structure (*i.e.*, dielectric 10) (*see, e.g.*, FIGs. 1-4; col. 2, lines 29-36), includes a first conductive layer 11 and a second conductive layer 12. The first conductive layer 11 of the finished fuse may be formed from aluminum or tungsten (col. 2, lines 43-45) and includes two spaced apart end regions (FIG. 3). The second conductive layer 12 of the fuse may be formed from the same material as the first layer 11 or from polysilicon. Col. 2, lines 59-63. In a finished fuse, such as that illustrated in FIG. 3 of Fischer, end portions of the second conductive layer 12 overlie the spaced apart regions of the first conductive layer 11, while the central portion 111 of the second conductive layer 12 is located in substantially the same plane as the first conductive layer 11 and between the spaced apart portions of the first conductive layer 11. *See also,* col. 2, lines 56-58.

Fischer teaches that the fuse may be fabricated by forming a first layer of conductive material 11 over an insulative structure 10 (FIG. 1; col. 2, lines 45-48), patterning a "window" 111 in the first layer of conductive material to expose a portion of the underlying insulative structure (FIG. 1; col. 2, lines 36-38; col. 3, lines 34-55), forming a second layer 12 of conductive material over the first layer 11 and within the window 111 (FIG. 2; col. 2, lines 49-55), and patterning the "combined" first and second layers to form the fuse (FIG. 3; col. 2, lines 56-58).

By patterning the first conductive layer is this manner, laterally discrete spaced apart regions, such as regions 14a and 14b described in the examples of the above-referenced application, are not formed. Instead, the majority of the patterned layer 11 remains, with small windows 111 being formed therethrough.

Chen

Chen likewise teaches a fuse and a method for fabricating the fuse. The fuse of Chen may be formed from aluminum, titanium tungsten, a silicide or polycide, or polysilicon. Col. 5, lines 59-63, but only includes a single material layer.

A portion of the fuse described in Chen is exposed by way of a so-called fuse "window." *See, e.g.,* col. 4, lines 50-54. This "window" facilitates programming of the fuse with a laser. *See* col. 7, lines 38-40. In order to prevent contamination of the fuse prior to programming thereof, as well as to prevent contamination of the underlying semiconductor device features following programming of the fuse, Chen teaches a method for forming a moisture barrier both above and beneath the window of the fuse.

Mitani

Mitani teaches a fuse with lower layer that is formed from polycrystalline silicon and an upper layer with spaced apart regions that are formed from a metal silicide, as well as methods for fabricating such a fuse. Mitani, Abstract. In the fabrication method, the polycrystalline silicon is first deposited on a field oxide. *Id.* Next, a layer of metal silicide is formed over the

polycrystalline silicon, and the layers are etched in combination. *Id.* Finally, the intermediate part of the metal silicide is etched, leaving only polycrystalline silicon as the central region of the finished fuse, the portion of the fuse that is to be ruptured. *Id.*

Sandhu

Sandhu teaches a process for depositing a tungsten silicide film on a substrate using chemical vapor deposition.

Degelormo

Degelormo merely teaches a chemical vapor deposition method for forming layers of conductively doped polysilicon. Degelormo includes no teaching or suggestion that the CVD process thereof may be used to fabricate any part of a fuse or structures associated directly with a fuse, let alone laterally discrete, spaced apart regions comprising polysilicon over an insulative structure around and between which an underlying insulative structure is exposed.

Ukeda

Ukeda teaches a dry etch process for anisotropically removing exposed regions of a polysilicon layer through a metal silicide layer. Ukeda does not teach or suggest that the process disclosed therein may be used in fabricating a fuse.

(3) Reasoning

(a) Claims 17, 19-24, and 26-33

Claims 17, 19-24, and 26-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer in view of Chen.

There are several reasons that a *prima facie* case of obviousness has not been established with respect to the subject matter recited in claims 17, 19-24, and 26-33.

One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Asserted Combination

First, one of ordinary skill in the art would not have been motivated to combine the teachings of Fischer and Chen in the manner that has been asserted in the outstanding Office Action.

Specifically, Fisher does not provide any motivation to one of ordinary skill in the art to form one of the fuse layers taught therein from a metal silicide. Chen does not provide one of ordinary skill in the art with any motivation to use a multi-layer fuse in place of the single-layer fuse taught therein. As neither of these references nor the knowledge that was generally available in the art prior to the filing date of the above-referenced application provides any suggestion of the desirability of forming a fuse with multiple layers, one of which comprises a metal silicide, another of which comprises metal or polysilicon, none of Fischer, Chen, or the knowledge that was generally available in the art before the filing date of the above-referenced application would have motivated one of ordinary skill in the art to make the asserted combination.

Moreover, by touting the usefulness of aluminum, tungsten, or polysilicon for use in forming the programmable portion of the fuse described therein, Fischer teaches away from the asserted motivation to use a metal silicide as a programmable portion of a fuse.

Further, Fischer teaches methods for fabricating a fuse which is configured to be blown by an electrical current, while the teachings of Chen are limited to a method for fabricating a fuse which is configured to be blown with a laser beam.

As such motivation to combine reference teachings is obviously lacking, the rejection of claims 17, 19-24, and 26-33 appears to be based entirely and improperly upon hindsight gleaned from the teachings of the above-referenced application.

The Asserted Combination Does Not Teach or Suggest Each and Every Claim Element

Second, the asserted combination of Fischer and Chen does not teach or suggest each and every element of independent claim 17.

Independent claim 17 of the above-referenced application recites a method for fabricating a fuse. The method of claim 17 includes, among other things, patterning a layer of conductive material to define at least two laterally distinct, spaced apart regions, between and around which an underlying insulative structure is exposed. The method of claim 17 also includes disposing a layer of metal silicide over and between the two regions of conductive material.

In contrast to the subject matter recited in independent claim 17, Fischer and Chen *both* lack any teach or suggestion of patterning a conductive layer to define at least two laterally distinct, spaced apart regions between and around which an underlying insulative structure is

exposed. Instead, the teachings of Fischer are limited to forming windows in a lower layer of conductive material, then covering the lower layer of conductive material and filling the windows with another, upper layer of conductive material before defining laterally discrete regions from the lower layer of conductive material. Thus, when the method of Fischer is employed, an insulative structure which underlies the lower layer of conductive material cannot be exposed both around and between the spaced apart regions as the spaced apart regions are formed therein.

Chen teaches forming an entire fuse from a single layer of conductive material, thus, Chen does not teach or suggest forming laterally spaced apart regions of a fuse from a layer of conductive material.

The assertion at page 18 of the Final Office Action dated August 21, 2002, that the references have been "attack[ed] individually where the rejections are based on combinations of references . . ." is not understood, since substantially the same argument has been maintained throughout prosecution of the above-referenced application–that *both* Fischer and Chen lack any teaching or suggestion of forming laterally discrete, spaced apart regions from a layer of conductive material between and around which an underlying insulative structure is exposed.

As Fischer *and* Chen both fail to provide any teaching or suggestion of this element of independent claim 17, these references cannot together teach or suggest the method which is recited in independent claim 17.

As Fischer and Chen, *taken together,* fail to teach or suggest all of the elements of independent claim 17, they also fail to teach or suggest each and every element of claims 19-24 and 26-33, each of which depends either directly or indirectly from claim 17.

No Reasonable Expectation of Success

Third, one of ordinary skill in the art would have no reason to believe that combining the teachings of Fischer and Chen could result in the method which is recited in independent claim 17, or in the methods of any of claims 19-24 or 26-33. This is because one of ordinary skill in the art would readily recognize that since neither Fischer nor Chen teaches or suggests a method which includes "patterning [a] layer of conductive material" in such a way as "to define at least two laterally discrete, spaced apart regions of conductive material" therefrom, "between and around" which an underlying insulative structure is exposed, there is no reason to expect that combining the teachings of Fischer and Chen would result in the method which is recited in independent claim 17.

For these reasons, a *prima facie* case of obviousness of claims 17, 19-24, and 26-33 has not been established pursuant to the requirements of 35 U.S.C. § 103(a). Therefore, claims 17, 19-24, and 26-33 are allowable over the combination of Fischer and Chen. Accordingly, the rejection of claims 17, 19-24, and 26-33 should be reversed.

(b) Claim 18

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer and Chen and, further, in view of Mitani.

Claim 18 is allowable, among other reasons, as depending from claim 17, which should be allowed.

Moreover, Mitani does not remedy the deficiencies that have been noted previously herein with respect to the asserted combination of Fischer and Chen.

One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Asserted Combination

One of ordinary skill in the art would not have been motivated to combine the teachings of Mitani with those of Fischer or Chen in the manner that has been asserted in the outstanding office action.

The teachings of Fischer are limited to methods for fabricating a multi-layer fuse, with none of the layers comprising metal silicide. Nor does Fischer provide one of ordinary skill in the art with any motivation to use metal silicide to form one of the layers of the fuse described therein. Chen teaches a method for forming a single-layer fuse from a variety of materials, including metal silicide, but does not provide one of ordinary skill in the art with any motivation to also use another conductive material and, thus, multiple layers at the ends, or terminals, of the fuse. While Mitani includes the combined use of a metal silicide layer with a polysilicon layer, Mitani teaches that the metal silicide, not the polysilicon, is patterned to form discrete, spaced apart regions and, thus, that the polysilicon, not the metal silicide, is useful for forming the region of the fuse which is to be ruptured.

As such, one of ordinary skill in the art would not have been motivated to combine the teachings of Mitani with those of either Fischer or Chen. This is because Fisher teaches forming a two-layer fuse with the upper layer forming the region of a fuse which is configured to be

blown, while Mitani teaches forming a two-layer fuse with the lower layer of the resulting fuse being configured to be blown. Further, neither Fischer nor Mitani teaches or suggests a method for fabricating a fuse that includes a metal silicide layer which is configured to be blown. Chen does not teach a fuse fabrication method which includes forming and patterning multiple layers of conductive material.

There is also no motivation to combine the teachings of Chen with those of either Fischer or Mitani. This is because Fischer and Mitani teach the use of multiple layers to for a fuse, while Chen merely teaches the use of a single material layer. Moreover, Fischer and Mitani both teach the use of conventional materials to form the portion of a fuse that is configured to be blown, while Chen teaches that metal silicide may be used to form the portion of a fuse which is to be blown. Further, Fischer and Mitani teach methods for fabricating fuses which are configured to be blown by an electrical current, while the teachings of Chen are limited to methods for fabricating fuses that are configured to be blown with laser beams.

For these reasons, one of ordinary skill in the art would not be motivated, either by the teachings of Fischer, Chen, and Mitani, or by the knowledge that was available to one or ordinary skill in the art prior to the filing date of the above-referenced application, to combine the teachings of Fischer, Chen, and Mitani in the manner that has been asserted.

Any such motivation could only have been improperly gleaned from the hindsight which the description of the above-referenced application provides.

The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element

With respect to the fuse fabrication process described in Mitani, there is no teaching or suggestion of patterning a conductive layer, such as the polysilicon layer thereof, to form at least two laterally discrete, spaced apart regions between and around which regions of an underlying insulative structure are exposed. As this teaching is also lacking in both Fischer and Chen, the combination of Fischer, Chen, and Mitani cannot teach or suggest these elements.

There Is No Reasonable Expectation that the Proposed Combination Would Be Successful

One of ordinary skill in the art would not have any reason to expect that combining the methods described in Fischer, Chen, and Mitani would result in the method that is recited in claim 18. This is primarily due to directive provided in M.P.E.P. § 2141.02 that, in combining reference teachings, the teachings of the references must be considered in their entireties. Due to the extreme divergence between the methods of Fischer, Chen, and Mitani, there is no way all of the teachings of these references could be considered in developing a fuse fabrication method such as to which claim 18 is limited. The most likely result of such a combination would resemble the method taught in Mitani, without removal of material of the metal silicide layer from the region of the fuse which is configured to rupture during patterning of the metal silicide layer.

Furthermore, as none of Fischer, Chen, or Mitani teaches or suggests forming laterally discrete, spaced apart regions from a layer of conductive material between and around which an underlying insulative structure is exposed, as recited in claim 17, from which claim 18 depends,

there is no way that one of ordinary skill in the art would have a reasonable expectation that the asserted combination of teachings from Fischer, Chen, and Mitani could result in the method which is recited in claim 18.

The foregoing illustrates a few of the reasons why a *prima facie* case of obviousness has not been established against claim 18 under 35 U.S.C. § 103(a). As a *prima facie* case of obviousness has not been set forth, claim 18 is allowable over the combination of Fischer, Chen, and Mitani. Therefore, reversal of the 35 U.S.C. § 103(a) rejection of claim 18 is respectfully requested.

(c) Claim 25

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer and Chen and, further, in view of Sandhu.

Claim 25 is allowable, among other reasons, as depending from claim 17, which should be allowed. Claim 25 is further allowable since Sandhu, which merely teaches a process for depositing a tungsten silicide film by chemical vapor deposition, does not provide any teaching or suggestion which remedies the aforementioned deficiencies in the asserted combination of Fischer and Chen.

(d) Claims 50, 51, 55-60, and 62-68

Claims 50, 51, 55-60, and 62-68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer in view of Mitani and Chen.

The reasons that one of ordinary skill in the art would not have been motivated to combine the teachings of these references in the asserted manner and the reasons that one of ordinary skill in the art would have not reason to expect the asserted combination to be successful have been set forth above.

The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element

Moreover, none of Fischer, Mitani, or Chen teaches or suggests each and every element of claims 50, 51, 55-60, and 62-68. Accordingly, the combination of Fischer, Mitani, and Chen cannot teach or suggest each and every element of any of claims 50, 51, 55-60, or 62-68.

Independent claim 50 recites a method for fabricating a fuse that includes, among other things, fabricating laterally discrete, spaced apart regions comprising polysilicon on an insulative structure and fabricating a fuse comprising a metal silicide. When the laterally discrete, spaced apart regions are fabricated and prior to forming the overlying fuse, an underlying insulative structure is exposed between and around the spaced apart regions. The fuse is fabricated in such a way as to include a central region disposed adjacent to the insulative structure and between the spaced apart regions, as well as at least two terminal regions over the spaced apart regions and on opposite ends of the central region.

The teachings of Fischer are limited to forming a window centrally through a conductive layer, which could not result in laterally discrete, spaced apart regions of a first layer of conductive material. When the second conductive layer is formed, the insulative structure is no longer exposed through the window. According to Fischer, the first layer of conductive material is not patterned to form laterally discrete, spaced apart regions until after the second layer of conductive material has been formed and covers any portions of the insulative structure that were previously exposed through the window.

Moreover, in the method taught by Fischer, the insulative structure that underlies the conductive structure is not exposed both between and around the laterally discrete, spaced apart regions prior to the fabrication of a fuse thereover.

Further, Fischer teaches that polysilicon may be used to form a top layer of the fuse described therein, including the fusible element that extends between terminals of the fuse. There is no teaching or suggestion in Fischer, however, that spaced apart regions may be formed from polysilicon.

Mitani also lacks any teaching or suggestion of a method that includes fabricating spaced apart regions from polysilicon, with an underlying insulative structure being exposed both between and around the spaced apart regions as they are fabricated. Instead, the spaced apart regions of Mitani are formed from a metal silicide and located over a conductive structure. The underlying field oxide structure is never exposed between the metal silicide spaced apart regions of Mitani. Additionally, Mitani neither teaches or nor suggests fabricating a fuse that comprises

metal silicide and that includes a central region disposed adjacent to an insulative structure and between spaced apart regions that comprise polysilicon.

Chen lacks any teaching or suggestion of fabricating spaced apart regions from any type of conductive material, let alone polysilicon. Nor does Chen teach or suggest that, in fabricating the metal silicide fuse taught therein, a central region of the fuse is disposed between spaced apart regions that comprise polysilicon.

Taken together, it is clear that none of Fischer, Mitani, or Chen teaches or suggest fabricating laterally discrete, spaced apart regions that comprise polysilicon, that an insulative structure is exposed both between and around such spaced apart regions as they are formed, or fabricating a fuse that comprises a metal silicide with a central region thereof disposed between such spaced apart regions.

For these reasons, the asserted combination of Fischer, Mitani, and Chen cannot support a *prima facie* case of obviousness, pursuant to 35 U.S.C. § 103(a), against independent claim 50. Therefore, under 35 U.S.C. § 103(a), independent claim 50, as well as each of claims 51, 55-60, and 62-68, which depend either directly or indirectly from claim 50, are allowable over Fischer, Mitani, and Chen. Accordingly, the 35 U.S.C. § 103(a) rejection of claims 50, 51, 55-60, and 62-68 should be reversed.

(e) Claims 52-54, 69, and 70

Claims 52-54, 69, and 70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer, Mitani, and Chen and, further, in view of Degelormo.

The teachings of Fischer, Mitani, and Chen have been summarized previously herein.

As Degelormo merely teaches a chemical vapor deposition method for forming layers of conductively doped polysilicon without teaching or suggesting that the CVD process thereof may be used to fabricate any part of a fuse or structures associated directly with a fuse, let alone laterally discrete, spaced apart regions comprising polysilicon over an insulative structure around and between which an underlying insulative structure is exposed, Degelormo includes no teaching or suggestion that would remedy the deficiencies of Fischer, Mitani, and Chen with respect to their inabilities to have provided one of ordinary skill in the art with motivation to make the asserted combination.

Nor do the teachings of Degelormo provide one of ordinary skill in the art with any additional reason to believe that the teachings of Fischer, Mitani, Chen, and Degelormo could be successfully combined to provide a method for fabricating a fuse. In particular, Degelormo does not include any teaching or suggestion of "fabricating laterally discrete, spaced apart regions comprising polysilicon on an insulative structure of a semiconductor device, said insulative structure being exposed between and around each of said spaced apart regions", an element of the fuse fabrication process recited in claim 50, from which claims 52-54, 69, and 70 depend, which is also missing from Fischer, Mitani, and Chen.

Furthermore, claims 52-54, 69, and 70 are each allowable, among other reasons, as depending from claim 50, which is allowable.

Therefore, under 35 U.S.C. § 103(a), claims 52-54, 69, and 70 are allowable over the combination of Fischer, Mitani, Chen, and Degelormo. As such, it is respectfully requested that the 35 U.S.C. § 103(a) rejection of claims 52-54, 69, and 70 be reversed.

(f) Claim 61

Claim 61 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer, Mitani, and Chen and, further, in view of Sandhu.

As explained previously herein, Sandhu does not provide any teaching or suggestion that remedies the deficiencies that have been identified herein with respect to the asserted combination of Fischer and Chen. For the same reasons, as well as those discussed previously herein with respect to the asserted combination of Fischer, Mitani, and Chen, Sandhu would not remedy the deficiencies that have been noted regarding the asserted combination of Fischer, Mitani, and Chen. Therefore, a *prima facie* case of obviousness cannot be established against claim 61 based merely upon the asserted combination of teachings from Fischer, Mitani, Chen, and Sandhu.

Claim 61 is allowable, among other reasons, as depending from claim 50 and 60, which are allowable.

(g) Claims 71, 74-86, 88-96, and 101

Claims 71, 74-86, 88-96, and 101 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mitani in view of Fischer and Chen.

Independent claim 71 recites a method of fabricating a gate and a fuse that includes patterning regions of a layer of polysilicon to form laterally discrete, spaced apart regions of polysilicon around and between which an underlying field oxide region is exposed.

For the same reasons provided previously herein, one of ordinary skill in the art would not have been motivated to combine the teachings of Mitani, Fischer, and Chen. Moreover, for reasons presented previously herein, one of ordinary skill in the art would have no reason to believe that combining the teachings of these references would result in the method recited in claims 71, 74-86, 88-96, and 101 of the above-referenced application.

The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element

Further, the combined teachings of Mitani, Fischer, and Chen do not teach or suggest each and every element of independent claim 71.

Specifically, none of Mitani, Fischer, or Chen teaches or suggests a fuse fabrication method that includes "patterning at least regions of [a] layer of polysilicon disposed over at least one field oxide region . . . to define at least two laterally discrete, spaced apart regions from said polysilicon over said at least one field oxide region with portions of said at least one field oxide region being exposed laterally around each of said spaced apart regions and therebetween" or "disposing a layer of metal silicide on said layer of polysilicon and into contact with said [exposed] portions of said at least one field oxide region".

Instead, in the fabrication method of Mitani, the polysilicon layer is not patterned until after the metal silicide layer has been formed thereover. Moreover, as the metal silicide layer is

formed over the polyslicon layer prior to patterning of either layer, the metal silicide layer does not contact the field oxide region. Further, at no point is the field oxide region of Mitani exposed both laterally around and between portions of the polysilicon layer.

Chen neither teaches nor suggests disposing multiple layers to fabricate a fuse, nor patterning such layers. Thus, Chen does not teach or suggest forming a fuse by forming laterally discrete, spaced apart regions of a layer of conductive material prior to the formation of a second layer of conductive material.

The teachings of Fischer are limited to forming a window centrally through a conductive layer, which could not result in laterally discrete, spaced apart regions of a first layer of conductive material around and between which an underlying field oxide region is exposed. According to Fischer, no laterally discrete, spaced apart regions of the first layer of conductive material are formed until after the second layer of conductive material has been formed.

As none of Mitani, Chen, or Fischer teaches or suggests patterning at least regions of a layer of polysilicon in the manner recited in independent claim 71, any combination of these references also fails to teach or suggest this element of claim 71.

Claims 74-86, 88-96, and 101 are allowable, among other reasons, as depending either directly or indirectly from independent claim 71, which is allowable.

For these reasons, a *prima facie* case of obviousness cannot be established based on the teachings of Mitani, Chen, and Fischer. Therefore, the 35 U.S.C. § 103(a) rejection of claims 71, 74-86, 88-96, and 101 should be reversed.

(h) Claim 72

Claim 72 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mitani, Fischer and Chen and, further, in view of Degelormo.

Claim 72 is allowable, among other reasons, as depending from claim 71, which should be allowed.

(i) Claim 87

Claim 87 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mitani, Fischer and Chen and, further, in view of Sandhu.

Claim 87 is allowable, among other reasons, as depending from claim 71, which should be allowed.

(j) Claims 97-100

Claims 97-100 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mitani, Fischer and Chen and, further, in view of Ukeda.

Ukeda teaches a dry etch process for anisotropically removing exposed regions of a polysilicon layer through a metal silicide layer. Ukeda does not teach or suggest that the process disclosed therein may be used in fabricating a fuse.

Accordingly, it is clear that Ukeda does not remedy the deficiencies of Mitani, Chen, and Fischer, and the knowledge that was generally available in the art prior to the filing date of the above-referenced application with respect to providing some motivation to one of ordinary skill

in the art to combine the teachings of these references. It is also clear that Ukeda does not include any teaching that would give one of ordinary skill in the art a reasonable basis for expecting the combination of Mitani, Chen, Fischer, and Ukeda to provide a successful method for fabricating a fuse.

Claims 97-100 are each allowable, among other reasons, as depending from claim 71, which should be allowed.

Accordingly, reversal of the 35 U.S.C. § 103(a) rejections of claims 97-100 is respectfully requested.

(9) APPENDICES

A copy of claims 17-33, 50-72, and 74-101 is appended hereto as "Appendix A."

(10) CONCLUSION

It is respectfully submitted that:

(A) The drawings of the above-referenced application comply with the requirements of 37 C.F.R. § 1.121(a)(6) by depicting subject matter which is supported by the specification which was originally filed in the above-referenced application;

(B) The drawings of the above-referenced application comply with the requirements of 37 C.F.R. § 1.83(a) by depicting subject matter which is recited in the claims;

(C) The specification of the above-referenced application provides proper antecedent basis for the subject matter recited in the claims, in compliance with 37 C.F.R. § 1.75(d)(1) and M.P.E.P. § 608.01(o);

(D) Claims 17-33, 50-72, and 74-101 are allowable under 35 U.S.C. § 112, first paragraph, for describing the inventive subject matter in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention;

(E) Claims 17, 19-24, and 26-33 are allowable under 35 U.S.C. § 103(a) over Fischer and Chen;

(F) Claim 18 recites subject matter which is allowable under 35 U.S.C. § 103(a) over Fischer, Chen, and Mitani;

(G) Claim 25 is allowable under 35 U.S.C. § 103(a) as reciting subject matter which is patentable over Fischer, Chen, and Sandhu;

(H) Claims 50, 51, 55-60, and 62-68 are allowable under 35 U.S.C. § 103(a) as reciting subject matter which is allowable over Fischer, Mitani, and Chen;

(I) Claims 52-54, 69, and 70 recite subject matter which is patentable under 35 U.S.C. § 103(a) over Fischer, Mitani, Chen, and Degelormo;

(J) Claim 61 is allowable for reciting subject matter which, under 35 U.S.C. § 103(a), is patentable over Fischer, Mitani, Chen, and Sandhu;

(K) Claims 71, 74-86, 88-96, and 101 are allowable under 35 U.S.C. § 103(a) as being patentable over Mitani, Fischer, and Chen;

(L) Claim 72 is patentable, under 35 U.S.C. § 103(a), for reciting subject matter which is allowable over the combination of Mitani, Fischer, Chen, and Degelormo;

(M) Claim 87 recites subject matter which is patentable under 35 U.S.C. §103(a) over Mitani, Fischer, Chen, and Sandhu; and

(N) Claims 97-100 recite subject matter which is patentable under 35 U.S.C. § 103(a) as being nonobvious over Mitani, Fischer, Chen, and Ukeda.

Accordingly, reversal of the objections to the drawings and specification, as well as of the rejections of claims 17-33, 50-72, and 74-101 under both 35 U.S.C. § 112, first paragraph, and 35 U.S.C. § 103(a) is respectfully solicited.

Respectfully submitted,

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APPENDIX A

17. A method of fabricating a fuse upon a semiconductor device, comprising:

disposing a.layer of conductive material over an insulative structure of the semiconductor device;

patterning said layer of conductive material to define at least two laterally discrete, spaced apart regions of conductive material between and around which said insulative structure is exposed;

disposing a layer of metal silicide over the semiconductor device, including adjacent to said at least two regions and to said insulative structure exposed between and around said at least two regions; and

patterning said layer of metal silicide so as to define at least two terminal regions of the fuse, each of which is in contact with a corresponding one of said at least two regions of conductive material, and a central region disposed between said at least two terminal regions and in contact with said insulative structure.

18. The method of claim 17, wherein said disposing said layer of conductive material comprises disposing polysilicon onto said insulative structure.

19. The method of claim 17, wherein said patterning said layer of conductive material comprises disposing a mask over the semiconductor device and removing selected regions of said layer of conductive material through said mask.

20. The method of claim 19, wherein said disposing said mask comprises:

disposing photoresist onto the semiconductor device;

exposing selected regions of said photoresist; and

developing said selected regions.

21. The method of claim 19, wherein said removing comprises etching said selected regions of said layer of conductive material through said mask.

22. The method of claim 21, wherein said etching comprises isotropically etching said selected regions.

23. The method of claim 21, wherein said etching comprises wet etching said selected regions of said layer of conductive material.

24. The method of claim 17, wherein said disposing said layer of conductive material comprises chemical vapor depositing said layer of conductive material.

25. The method of claim 17, wherein said depositing said layer of metal silicide comprises chemical vapor depositing said layer of metal silicide.

26. The method of claim 17, wherein said depositing said layer of metal silicide comprises depositing tungsten silicide.

27. The method of claim 17, wherein said patterning said layer of metal silicide comprises disposing a mask over the semiconductor device and removing selected regions of said layer of metal silicide through said mask.

28. The method of claim 27, wherein said disposing said mask comprises:

disposing photoresist over the semiconductor device;

exposing selected regions of said photoresist; and

developing said selected regions.

29. The method of claim 27, wherein said removing comprises etching said selected regions of said layer of metal silicide.

30. The method of claim 29, wherein said etching comprises anisotropically etching said selected regions of said layer of metal silicide.

31. The method of claim 29, wherein said etching comprises dry etching said selected regions of said layer of metal silicide.

32. The method of claim 17, further comprising disposing a contact in communication with at least one of said at least two terminal regions.

33. The method of claim 32, further comprising disposing another contact in communication with another of said at least two terminal regions.

50. A method of fabricating a fuse, comprising:

fabricating laterally discrete, spaced apart regions comprising polysilicon on an insulative structure of a semiconductor device, said insulative structure being exposed between and around each of said spaced apart regions; and

fabricating a fuse comprising a metal silicide, including a central region disposed adjacent the insulative structure and between said spaced apart regions and at least two terminal regions disposed on opposite ends of the central region and adjacent said spaced apart regions.

51. The method of claim 50, wherein said fabricating spaced apart regions comprises:

disposing polysilicon onto said insulative structure; and

patterning said polysilicon.

52. The method of claim 51, wherein said disposing polysilicon comprises chemical vapor depositing polysilicon.

53. The method of claim 51, further comprising doping said polysilicon.

54. The method of claim 53, wherein said doping occurs substantially simultaneously with said disposing.

55. The method of claim 51, wherein said patterning comprises disposing a mask adjacent said polysilicon and removing selected regions of said polysilicon through said mask.

56. The method of claim 55, wherein said disposing said mask comprises disposing photoresist adjacent said polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

57. The method of claim 55, wherein said removing selected regions of said polysilicon comprises etching said selected regions.

58. The method of claim 57, wherein said etching comprises isotropically etching said selected regions.

59. The method of claim 57, wherein said etching comprises wet etching said selected regions.

60. The method of claim 50, wherein said fabricating said fuse comprises disposing metal silicide adjacent said spaced apart regions and said insulative structure exposed therebetween.

61. The method of claim 60, wherein said disposing metal silicide comprises chemical vapor depositing metal silicide.

62. The method of claim 60, wherein said fabricating said fuse further comprises patterning said metal silicide.

63. The method of claim 62, wherein said patterning comprises disposing a mask adjacent said metal silicide and removing selected regions of said metal silicide through said mask.

64. The method of claim 63, wherein said disposing said mask comprises disposing photoresist adjacent said metal silicide, exposing selected regions of said photoresist, and developing said selected regions.

65. The method of claim 63, wherein said removing selected regions of said metal silicide comprises etching said selected regions of said metal silicide.

66. The method of claim 65, wherein said etching comprises anisotropically etching said selected regions.

67. The method of claim 65, wherein said etching comprises dry etching said selected regions.

68. The method of claim 62, wherein said patterning comprises defining said at least two terminal regions of the fuse adjacent said spaced apart regions and said central region of the fuse adjacent said insulative structure.

69. The method of claim 50, further comprising doping said spaced apart regions of polysilicon.

70. The method of claim 69, wherein said doping occurs substantially simultaneously with disposing polysilicon on said insulative structure.

71. A method of substantially simultaneously fabricating a gate and a fuse on a semiconductor substrate, comprising:

disposing a layer of insulative material over at least an exposed region of the semiconductor substrate;

disposing a layer of polysilicon over the semiconductor substrate, including over said layer of insulative material and over field oxide regions disposed on the semiconductor substrate;

patterning at least regions of said layer of polysilicon disposed over at least one field oxide region of said field oxide regions to define at least two laterally discrete, spaced apart regions from said polysilicon over said at least one field oxide region with portions of said at least one field oxide region being exposed laterally around each of said spaced apart regions and therebetween;

disposing a layer of metal silicide on said layer of polysilicon and into contact with said portions of said at least one field oxide region;

patterning at least said layer of metal silicide to define the fuse and the gate therefrom.

72. The method of claim 71, wherein said disposing said layer of polysilicon comprises chemical vapor depositing said layer of polysilicon.

74. (Previously amended) The method of claim 71, wherein said defining the fuse comprises defining a central region disposed adjacent and substantially between said at least two spaced apart regions and defining at least two terminal regions, each terminal region continuous

with an end of said central region and disposed adjacent one of said at least two spaced apart regions.

75. The method of claim 71, wherein said defining said at least two spaced apart regions comprises disposing a mask over said layer of polysilicon and removing selected regions of said layer of polysilicon through said mask.

76. The method of claim 75, wherein said disposing said mask comprises disposing photoresist over said layer of polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

77. The method of claim 75, wherein said removing comprises etching said layer of polysilicon.

78. The method of claim 77, wherein said etching comprises wet etching said layer of polysilicon.

79. The method of claim 77, wherein said etching comprises isotropically etching said layer of polysilicon.

80. The method of claim 71, further comprising patterning gate regions of said layer of polysilicon.

81. The method of claim 80, wherein said patterning said gate regions occurs substantially simultaneously with said patterning said at least regions of said layer of polysilicon.

82. The method of claim 80, wherein said patterning said gate regions comprises disposing a mask over said layer of polysilicon and removing selected regions of said layer of polysilicon through said mask.

83. The method of claim 82, wherein said disposing said mask comprises disposing photoresist over said layer of polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

84. The method of claim 82, wherein said removing comprises etching said selected regions.

85. The method of claim 84, wherein said etching comprises dry etching said selected regions.

86. The method of claim 84, wherein said etching comprises anisotropically etching said selected regions.

87. The method of claim 71, wherein said disposing said layer of metal silicide comprises chemical vapor depositing said layer of metal silicide.

88. The method of claim 71, wherein said defining the fuse and the gate from at least said layer of metal silicide comprises disposing a mask over said layer of metal silicide and removing selected regions of said layer of metal silicide through said mask.

89. The method of claim 88, wherein said disposing said mask comprises disposing photoresist over said layer of metal silicide, exposing selected regions of said photoresist, and developing said selected regions.

90. The method of claim 88, wherein said removing said selected regions comprises etching said selected regions.

91. The method of claim 90, wherein said etching comprises dry etching said selected regions.

92. The method of claim 90, wherein said etching comprises anisotropically etching said selected regions.

93. The method of claim 71, further comprising removing exposed regions of polysilicon through said layer of metal silicide.

94. The method of claim 93, wherein said removing comprises etching said exposed regions.

95. The method of claim 94, wherein said etching comprises dry etching said exposed regions.

96. The method of claim 94, wherein said etching comprises anisotropically etching said exposed regions.

97. The method of claim 93, further comprising removing exposed regions of said layer of insulative material through said layer of polysilicon.

98. The method of claim 97, wherein said removing said exposed regions of said layer of insulative material comprises etching said exposed regions of said layer of insulative material.

99. The method of claim 98, wherein said etching comprises dry etching said exposed regions of said layer of insulative material.

100. The method of claim 98, wherein said etching comprises anisotropically etching said exposed regions of said layer of insulative material.

101. The method of claim 71, further comprising doping at least one source region and at least one drain region of the semiconductor substrate, said at least one source region and said at least one drain region disposable adjacent the gate on opposite sides thereof.